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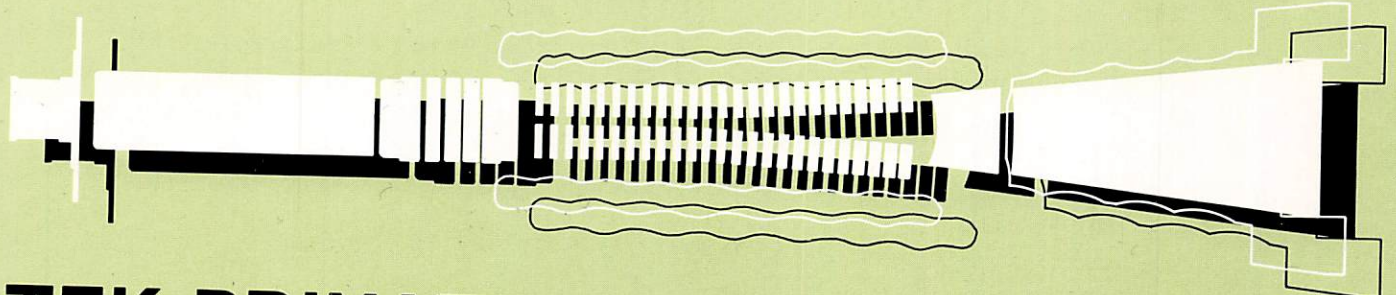
MAGNOLIA

Project Status Report

ARG Technical Memo No. CRG-TM-_____

Roger D. Bates

APPLIED RESEARCH TECHNICAL REPORT



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Computer Research
Applied Research Group
Tektronix Laboratories

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ABSTRACT

This document describes the status of this project after approximately six months of activity. It is intended to give a brief overview of the activity that has taken place over this period, as well as some idea of what remains to be done over the next 6 months.

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1. Summary of Goals

As a means of introduction, I would like to start with a very quick summary of the basic project goal. This is to implement a Single User System environment built up around the UNIX operating system and provide for high performance user interaction through the use of a multi-window bit-mapped display system.

As a means of attacking this problem the task has been broken down into two separate parts. The first is to bring up UNIX on a single processor system talking to the user through a conventional terminal via an RS232 connection. The second task is to implement a display sub-system utilizing the same basic processor talking to its own memory in order to build and maintain bit-mapped images for display on a high resolution monitor.

2. Current Activity

All activity up to this point has been centered around achieving the first of the two sub-goals mentioned above. Basically, all of the necessary hardware has been designed and constructed. Much of this hardware is tested and fully functional, while a few pieces still remain to be tested as the software tools become available to exercise them. The UNIX operating system has been re-written for the 68000 based processor system, and the code is just now being loaded into the system and the debugging phase has begun. A detail of the activities for each of the major areas of this project will be given in the last section of this report.

3. Future Activities

We are just now starting to address the second major task of this project - the requirements of the Bit-mapped display. The hardware portion of this task is fairly well defined. It will be to use the same processor board as used to support the operating system, connect it to its own memory board, and build a display controller capable of continually refreshing the monitor from the processor's memory.

The software portion of this task is much more complex, and will involve much more design effort before anything will be coded. We are just now beginning to address these issues. The basic issues revolve around determining what capabilities are to be implemented, where they are to be implemented (UNIX processor or Display processor), and how they will communicate.

4. Detailed Activities

4.1. Operating System - Clem Cole

At this time Steve Glaser and Clem Cole have succeeded in getting the basic UNIX kernel translated into a form that is more suitable for running on a 68000 Processor. At this time, the software is downloadable on the MAGNOLIA hardware and capable of initializing (except for memory sizing) and creating process 0 (the scheduler). After this, the machine attempts to create process 1 (the grand parent of all processes). It dies trying to access I/O (which it does not yet have).

We can currently demonstrate the kernel by making a pseudo process 0, that prints "Magnolia is running MAGIX". At this time, we are trying to correctly handle the traps, so that MAGIX can self-size memory. After that the Memory Management code will be written and real Disk I/O will be attempted.

Tom Merrow, Chip Schnarel and Clem have agreed on a disk protocol for getting I/O from the 11/44 to the Magnolia IOP. In this manner, we will set up the initial Magnolia's disk. Terry Loskodi will write the driver for the 11/44. Finally, Steve Glaser and Clem will create a program to "NUXI" the disk after putting the raw data out there.

4.2. Processor Board - Roger Bates

The hardware design is complete and stable. The board design involves implementing a system which is self-sufficient in its own right, that is the board contains 8k bytes of PROM, 2k bytes of RAM and its own RS232 port. The PROM is required for automatic start up of the system, while the RAM and terminal port are included purely for hardware and operating system debugging. The program in the PROM includes testing for all critical board resources, and support of a higher level debugging program which runs on a host processor. The start of such a debugging facility (mdb) is operational and runs on our 11/70 time shared UNIX environment. The program allows for down loading of Magnolia program, executing, interrupting and setting breakpoints in such a program. In addition, the state of the system, memory and internal 68000 registers may be examined and modified (using symbolic names for addresses).

A significant portion of the board is involved in the inter-processor communication (via the Object Bus). This portion of the board has not yet been tested. It is awaiting a suitable programming environment in which to run test programs, and a two processor configuration to test their interaction.

4.3. Memory Board - Ed Reuss

The first prototype memory board is presently up and running. The board is configured as follows;

- 256k bytes of RAM,
- using the Motorola 64k bit dynamic RAM ICs,
- accessible in 8 bit bytes, 16 bit words or 32 bit long words,
- with byte parity error detection.

The schematics for this board are up to date, and the board plus documentation are considered frozen.

A new board is being readied for CAD wire-wrap at this very moment. This new board will be logically and electrically identical to the first board. The only difference will be in the physical placement of the ICs on the board. This rearrangement was done in anticipation of the enhancements planned in the future (see below). The schematics for this board should be sent to CAD wire-wrap by the middle of the third week of May (week 20).

The next batch of blank prototyping boards is not expected to arrive until the first of June. When they arrive, the next memory board can be wire-wrapped. We expect to have that about the first week in June. An order has been placed for 40 memory parts for this board, with a scheduled shipping date of 25 May. This should be just about right with respect to the board availability.

Between now and the second week in June, when the next memory board should arrive, Ed will be finalizing the enhancements to the basic design for the "display memory board". These enhancements are basically designed and written down. The formal schematics need to be drawn and the parts placement on the board needs to be assigned. This board will then be submitted to CAD wire-wrap around the fourth week of May, and should be back about the fourth week in June.

4.3.1. Future plans

After June, an entire array of interesting tasks need to be addressed. They are identified below in order of importance.

- 512k byte memory board. This will double the capacity of the present board (256k). An additional eight or nine control ICs will be needed plus the obvious extra memory ICs. The present prototyping boards can easily accommodate the extra components.
- Custom memory control IC using gate array technology. The control and timing circuitry for the memory boards look like an excellent candidate for a custom gate array. This should reduce the part count and board space. It should also simplify the manufacture of the board making it less expensive to reproduce and debug.
- 1 Megabyte memory board. It is possible to get a 22 pin single in line package (SIP) with four memory parts and decoupling capacitors mounted onto a hybrid carrier. 32 of these packages plus 16 regular DIP packages (for parity) would allow us to make a 1 megabyte memory board. This could become the standard Magnolia

memory board. It might normally come with only 256k bytes installed. The customer could expand her memory at will by merely installing more parts up to the 1 megabyte maximum.

- Error correcting memory board. Users who feel they need error correction may wish to lobby for this option. At present, the 64k dynamic RAMs appear to be less susceptible to alpha particle induced soft errors than originally feared. The extra cost and complexity for ECC was considered unnecessary for a research environment. The IC designers are becoming more clever about reducing the problem and I expect that byte parity should be adequate for most of our applications for the near future. Some applications may find this unacceptable, but be prepared to suffer a 20% performance decrease for ECC memory.
- Error "sniffing" ECC memory board. Error sniffing is an extension of the ECC board listed above. In most dynamic memories, refresh is done by using a counter to select each "row" on the chip. The RAS line is asserted and all of the bits in that row are refreshed. For error sniffing, an extra counter is used to select each "column". A full fledged memory read cycle is performed, refreshing all of the bits in the selected row and error checking (with possible correcting, if necessary) on the selected row - column pair. A row - column pair is, by definition, a long word. This assures that each 256Kbyte board is completely error checked every half second.

The five options listed above pretty well sum up everything anyone would ever want in a Magnolia memory board for the next few years. If you have other ideas, don't be afraid to ask.

4.4. Memory Management Board - Roger Bates

This is a small subsystem (app 42 ic's) that are used to support the requirements of UNIX. This particular implementation provides for mapping of blocks of program address space into blocks of real memory through the use of "Base" and "Limit" registers (16 of each). This function has been placed on a separate board from the processor so that it may be omitted when not needed (the Display Processor), or replaced with a more sophisticated system (Virtual Memory) when required. The design is complete and a board fabricated, while testing should take place very shortly.

4.5. I/O Processor Board - Chip Schnarel, Merlin Miller

The IOP is the Input/Output Processor for the Magnolia personal computer system. The IOP contains a microcomputer to control the peripheral functions and two communications channels between the IOP and the Magnolia CPU.

This microcomputer has been checked out and is fully functional. This includes the check out of Z80 processor, memory, interrupt and peripheral decode logic.

The first of the two communications channels is the shared bus interface. It is a channel which allows the Magnolia CPU to read or write memory or peripherals on the IOP bus. It makes use of the bus control logic in the Z80. It is similar to a DMA interface. The shared bus interface has been through initial check out and works fine.

The second of the two communications channels is the gateway. The gateway provides a high speed DMA channel between the disk or network peripherals and the Magnolia memory. It is a bidirectional channel and can read or write either of the peripherals. The Local Bus can support up to a 32 bit wide data path. To make the most of each bus cycle the gateway is 32 bits wide on the local bus side. The peripherals require an 8 bit interface so the gateway is 8 bits wide on the peripheral side. The gateway does the conversion between 8 and 32 bits and has storage for up to five bytes internally. A subset of the gateway has been tested and works properly. This subset consists of the disk interface, the 8 to 32 bit conversion logic, the local bus address generation logic, and most of the control logic. The test reads or writes a sector on the disk and transfers it to or from Magnolia memory. The network interface (and associated control logic) are yet to be tested.

In addition to the communications channels and microcomputer, the IOP contains a number of useful peripherals and interfaces. These are all working properly at this time. The IOP has; 2 RS232c serial ports, 2 8 bit parallel ports, 8 ADC ports, 2 DAC ports, a clock/timer circuit, a crystal controlled calendar with battery back up, and a four voice sound generator. The network and disk interfaces are also accessible from the microcomputer. Speech synthesis is being considered as an additional IOP peripheral.

Several software test routines have been written to test the peripherals and interfaces. Also a monitor program has been written to make the IOP a stand alone computer. The monitor gives the user the capability to tie any input device to any output device. It will also connect together any two full duplex bidirectional peripherals. The monitor will accept commands from either RS232c port or the network. The IOP operating system, as defined by Rick Samco, has been written but not yet tested. The operating system when installed and functional will receive and execute commands given to it by the Magnolia CPU. These commands will send data to or gather data from the peripherals. The Magnolia CPU initiates execution of the IOP/OS, however if it fails to do so the IOP will execute the monitor instead. This function allows the user of a "dead" CPU to salvage disk files and/or peripheral data.

4.6. Mechanical Design / Technician Support - Ray Chase

At this point in time the schematics for the processor and memory boards are drawn and up to date with all mods and changes documented. The processor board is 75% debugged and the first pass on the memory card is complete. With the first memory card stable

and documentation complete Ed and Ray are working on a second version memory card which is a cleaner design using PALs, with construction projected for the first half of June. The memory management card has been implemented with the majority of the board being debugged using a raw schematic. The schematics will be redrawn into a formal state over the next few weeks.

Mechanical support for the project includes designing Magnolia's prototype board, extender card and backplane, which involved interfacing with the people at Walker Road. The additional items needed to create a completed unit are a card cage and sliding platform. The sliding platform will carry the disk drive, power supply plus the card cage and will reside inside the cabinet that will be used to house Magnolia.

The prototype cards have been designed and the first order of seven cards were received two months ago. Because of errors in fabrication only four of the seven could be made usable, but this was enough to build a minimum system. Since then the design has been enhanced and we are waiting for the second version negative to come back from CAD. When this occurs we will immediately order 20 additional boards and tighten the specs on fabrication. We are hoping to receive the new boards sometime during the first half of June. The card extender is designed and six cards have been made for us, with one currently in use. The design on the backplane has just been finished and it is currently in CAD being drawn up.

An initial card cage was designed and built several months ago and is now being used to support the first minimum configuration. The final design for the card cage is now in the model shop being fabricated. It will mate to the backplane currently being drawn at CAD.

Future mechanical activities will include the design and implementation of the sliding platform and any miscellaneous hardware needed to complete the project.